LCD Host LVDS Interface, Dual Pixel 20-112Mhz (SVGA/QXGA)

Overview:

V-Trans 's LVDS Display interface IP is based on National Semiconductor openLDI specification v0.95 dated May 13th 1999 that allow the transfer of digital display data between a display source and a display device.
The transmitter converts up to 48bits (single pixel 18bits, single pixel 24bits, dual pixel 18bits, dual pixel 24bits color) of CMOS data into 8 LVDS, (low voltage differential signaling) data streams.
Control signals (VSYNC, HSYNC, DE, and 2 user-defined signals) are sent along with the data stream in DC unbalance mode or during blanking intervals for DC balanced mode.
At a maximum dual pixel rate of 112Mhz, LVDS data line speed is 672Mbps, providing a total throughput of 5.38Gbps (672Megabytes per second).
DC balancing on a cycle-to-cycle basis as described by the openLDI specification is also provided to reduce ISI (Inter-Symbol Interference) in order to obtain a low distortion eye-pattern at the receiver end of the cable.

Features:

- 1P6M layout structure based on 0.18um 1P6M 1.8V generic logic process.
- 3.3V/1.8V ±10% supply voltage, -40/+125°C
- Complies with OpenLDI specification for digital display interfaces and LVDS IEEE Standard 1596.3-1996+ ANSI/TIA/EIA-644-A Specifications.
- Up to 5.38Gbps bandwidth
- DC Balance data transmission for low ISI distortion
- Dual pixel architecture supports interface to GUI and timing controller (dual/single pixel mode)
- Transmitter rejects cycle-to-cycle jitter
- Spread-spectrum input clock support
- Second LVDS clock for backward compatibility w/ FPD link
- Test mode with gray or PRBS patterns generator
- Core cell area : [contact us]
- Built-in power pads with ESD protection.
- Low leakage power-down mode <1uA.
- Reduced swing setting
- Equivalent part : National Semiconductor DS90C387

Block Diagram:

Deliverables:

V-Trans provides 2 separate kits depending on licensing agreement.
In most cases, the physical is merged on foundry site.

Design Kit

Design kit includes :

- LEF view and abstract gdsII
- Verilog HDL behavioral model
- Liberty (.lib) timing constraints for typical, worse and best corner case
- Full Datasheet /Application Note with integration guidelines document
- Silicon characterization report when available

Tapeout Kit

Tapeout kit includes the design kit plus plysical view:

- gdsII
- LVS netlist and report
- DRC/ERC/ESD/ANT report

Portfolio and Design Services:

V-Trans Microelectronics has been combining all the best practices and methodologies in analog and mixed-signal high speed interfaces design to answer the demanding market of high performance analog IPs using cheaper technologies such as 0.18um.

Our Portfolio covers a wide range of applications and can be customized on demand to answer exactly your specific needs.

Custom layout and back-end services are also available if you have a tied project schedule.
Our experience includes high integration circuit such as network SOC, CPU and FPGA which allow us to provide a full solution for even more complex chip.

Please contact us to tell us how we could help you or for any analog IP information.

- High speed interfaces (LVDS serdes, Display Interfaces, DDRII, DDR3, PCI-X, HDMI rev1.1)
- Converters (video ADC 10b 170Mhz, Triple video DAC)
- Timing circuits (Audio PLL, Video PLL, DDR memory PLL, custom PLL.)
- Low noise Crystal Oscillators
- Power management (LDO regulators, Power On Reset..)
- Video and WIMAX Analog Front end

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